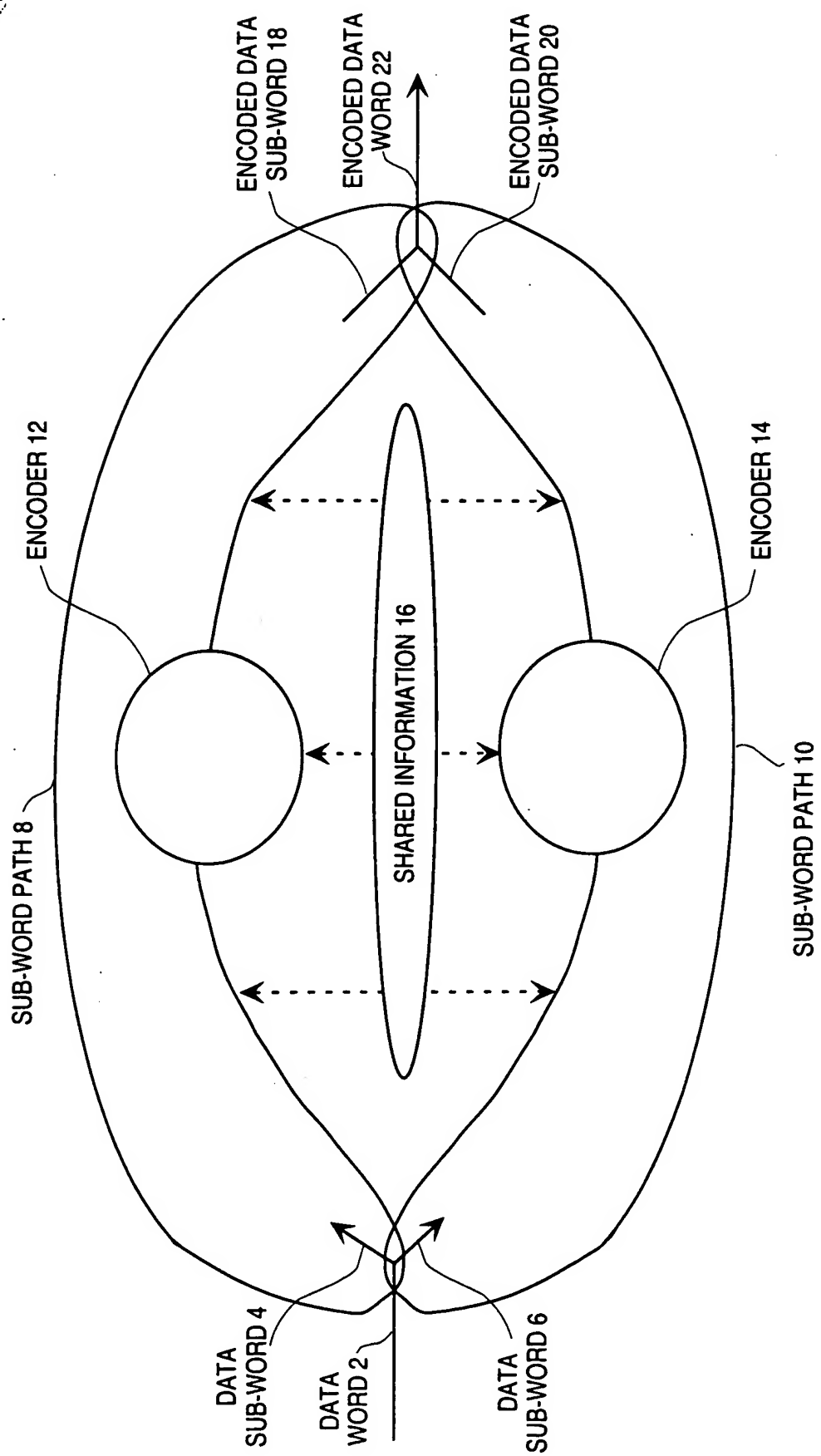


FIG. 1

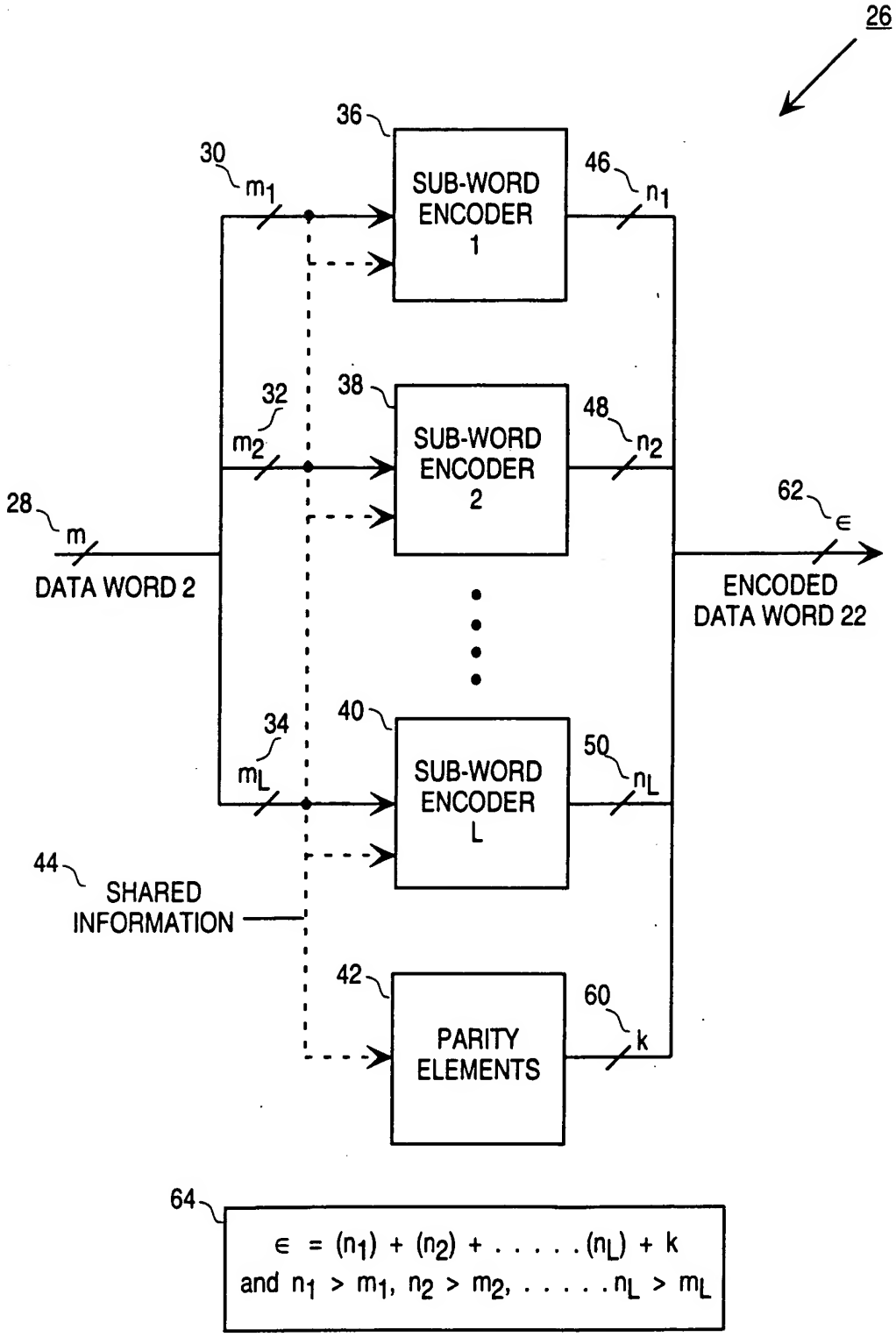

26
36
30
m_1
SUB-WORD ENCODER 1
46
n_1
32
38
m_2
SUB-WORD ENCODER 2
48
n_2
28
m
DATA WORD 2
62
ϵ
ENCODED DATA WORD 22
34
40
m_L
SUB-WORD ENCODER L
50
n_L
44
SHARED INFORMATION
42
PARITY ELEMENTS
60
k
64
$\epsilon = (n_1) + (n_2) + \ldots . (n_L) + k$
and $n_1 > m_1$, $n_2 > m_2$, $\ldots . n_L > m_L$

FIG. 2

FIG. 3

66

NUMBER OF ENCODED LINES (n)	p=0	p=1	p=2	p=3	p=4	p=5	p=6	p=7	p=8	p=9	p=10
n = 1	1.	1.									
n = 2	1.	2.	1.								
n = 3	1.	3.	3.	1.							
n = 4	1.	4.	6.	4.	1.						
n = 5	1.	5.	10.	10.	5.	1.					
n = 6	1.	6.	15.	20.	15.	6.	1.				
n = 7	1.	7.	21.	35.	35.	21.	7.	1.			
n = 8	1.	8.	28.	56.	70.	56.	28.	8.	1.		
n = 9	1.	9.	36.	84.	126.	126.	84.	36.	9.	1.	
n = 10	1.	10.	45.	120.	210.	252.	210.	120.	45.	10.	1.

NUMBER OF ONES (P) IN AN ENCODED WORD

FIG. 4

68

ENCODED WORD LENGTH	CODE STATES	INPUT WORD LENGTH	EXTRA LINES
3	2	1	2
4	6	2	2
5	10	3	2
6	20	4	2
7	35	5	2
8	70	6	2
9	126	6	3
10	252	7	3
11	462	8	3
12	924	9	3
13	1716	10	3
14	3432	11	3
15	6435	12	3
16	12870	13	3
17	24310	14	3
18	48620	15	3
19	92378	16	3
20	184756	17	3
21	352716	18	3

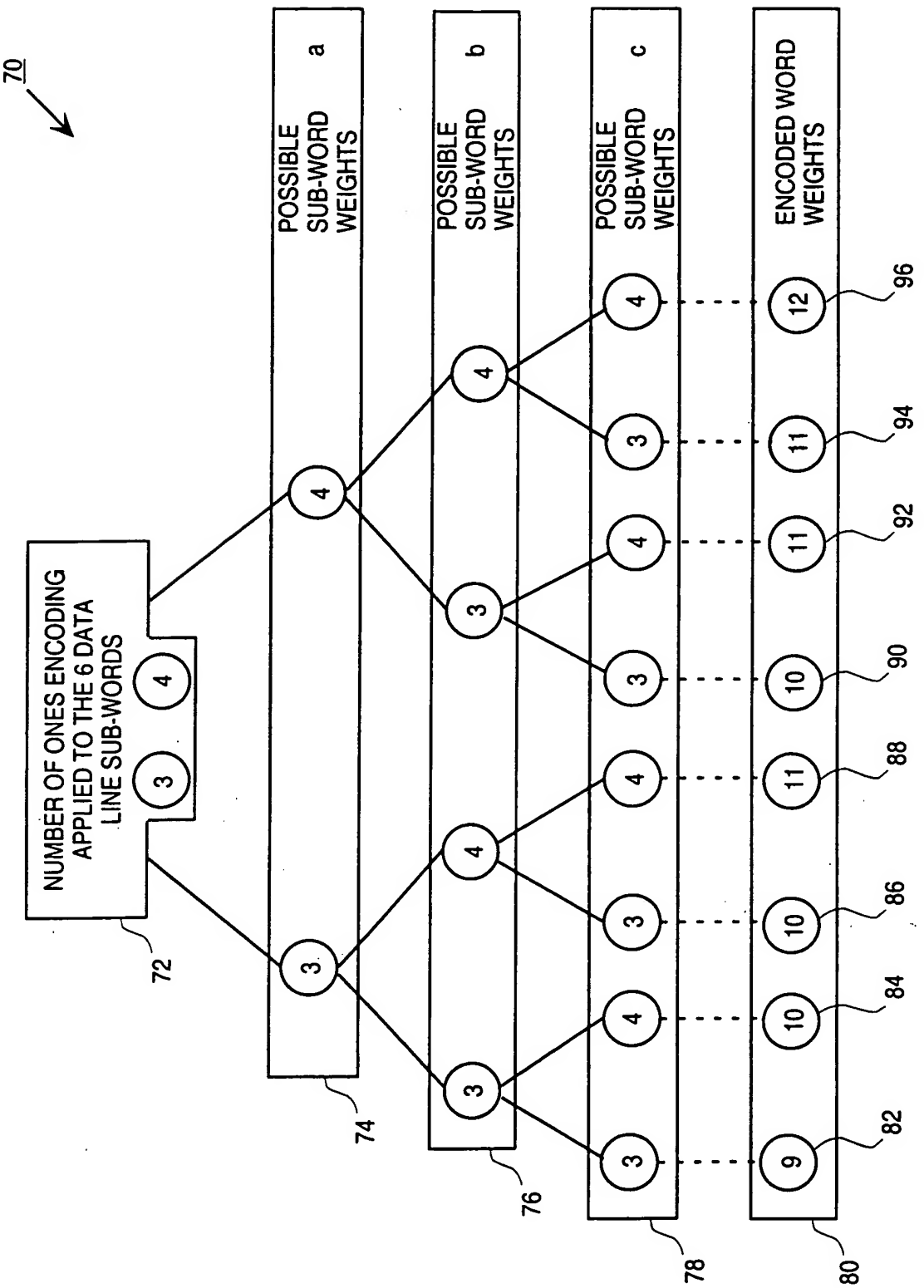

70
NUMBER OF ONES ENCODING APPLIED TO THE 6 DATA LINE SUB-WORDS
4
3
3
72
POSSIBLE SUB-WORD WEIGHTS a
4
3
74
POSSIBLE SUB-WORD WEIGHTS b
4
3
4
3
76
POSSIBLE SUB-WORD WEIGHTS c
4
3
4
3
4
3
78
ENCODED WORD WEIGHTS
12
11
11
10
11
10
10
9
80
96
94
92
90
88
86
84
82

FIG. 5

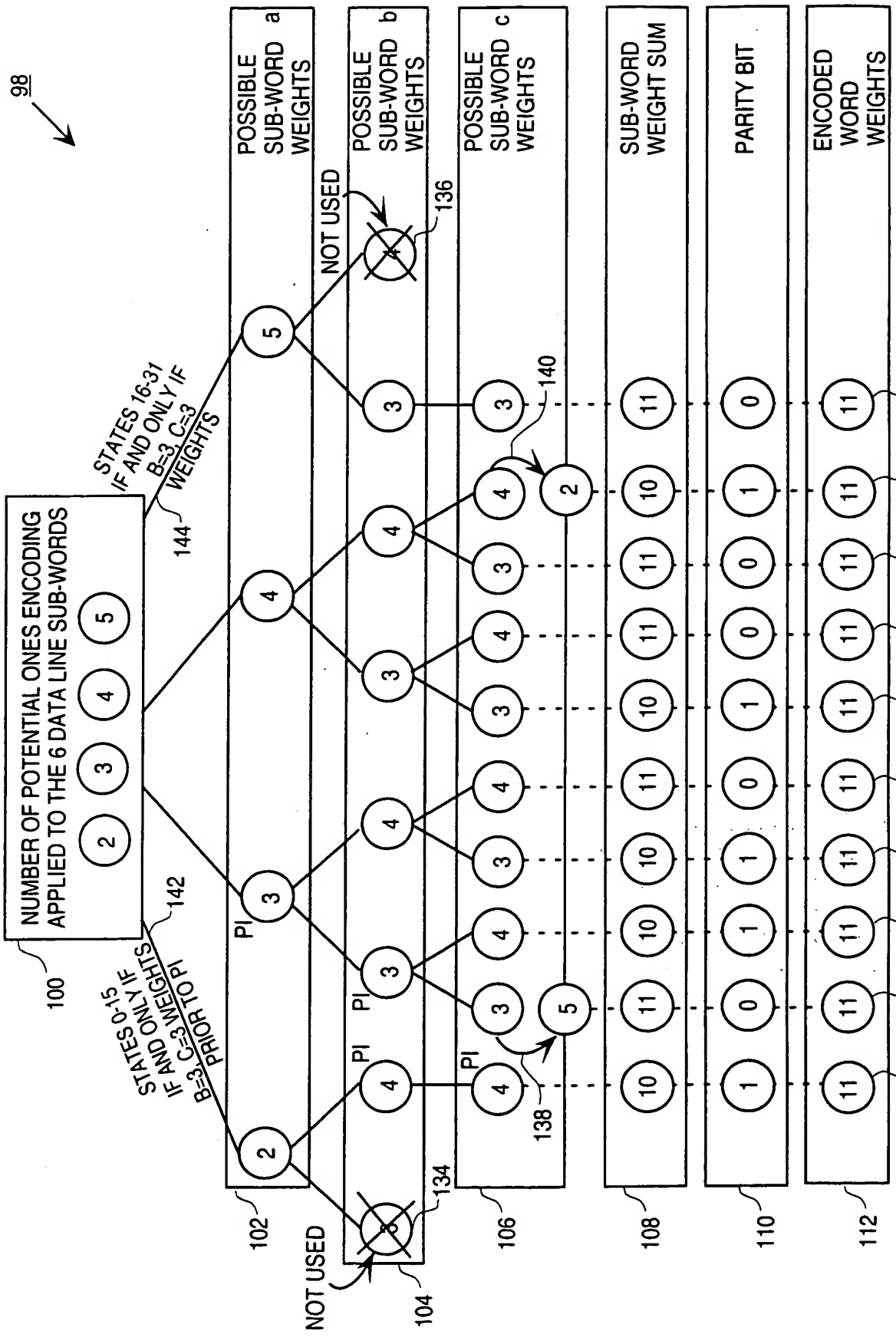

98
NUMBER OF POTENTIAL ONES ENCODING APPLIED TO THE 6 DATA LINE SUB-WORDS
2
3
4
5
100
STATES 0-15 IF AND ONLY IF B=3, C=3 WEIGHTS PRIOR TO PI
142
STATES 16-31 IF AND ONLY IF B=3, C=3 WEIGHTS
144
POSSIBLE SUB-WORD a WEIGHTS
POSSIBLE SUB-WORD b WEIGHTS
POSSIBLE SUB-WORD c WEIGHTS
SUB-WORD WEIGHT SUM
PARITY BIT
ENCODED WORD WEIGHTS
NOT USED
PI
102
104
106
108
110
112
134
136
138
140
114
116
118
120
122
124
126
128
130
132

FIG. 6

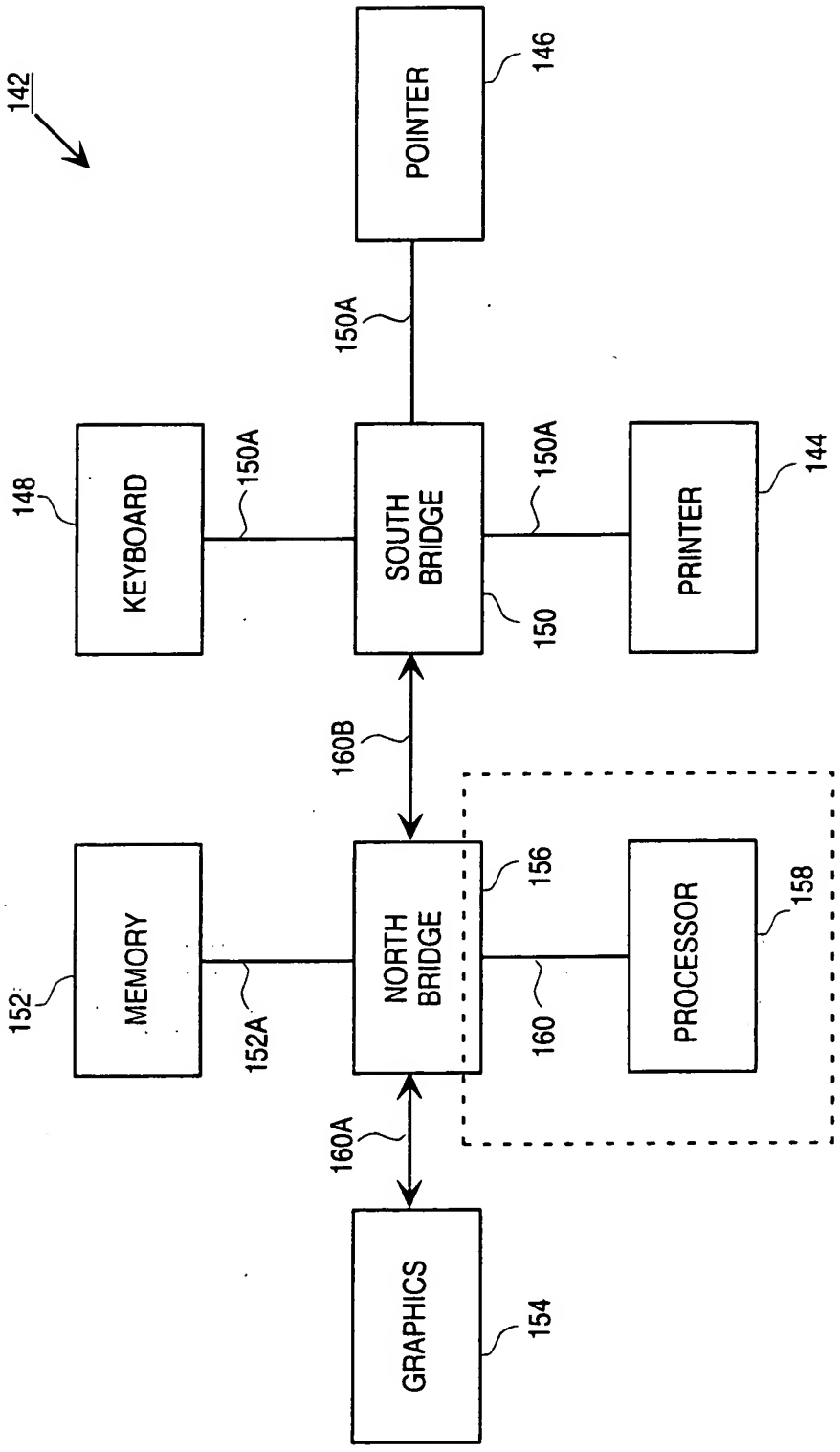

142
POINTER
146
150A
KEYBOARD
148
150A
SOUTH BRIDGE
150A
PRINTER
144
150
160B
MEMORY
152
152A
NORTH BRIDGE
156
PROCESSOR
158
160
160A
GRAPHICS
154

FIG. 7

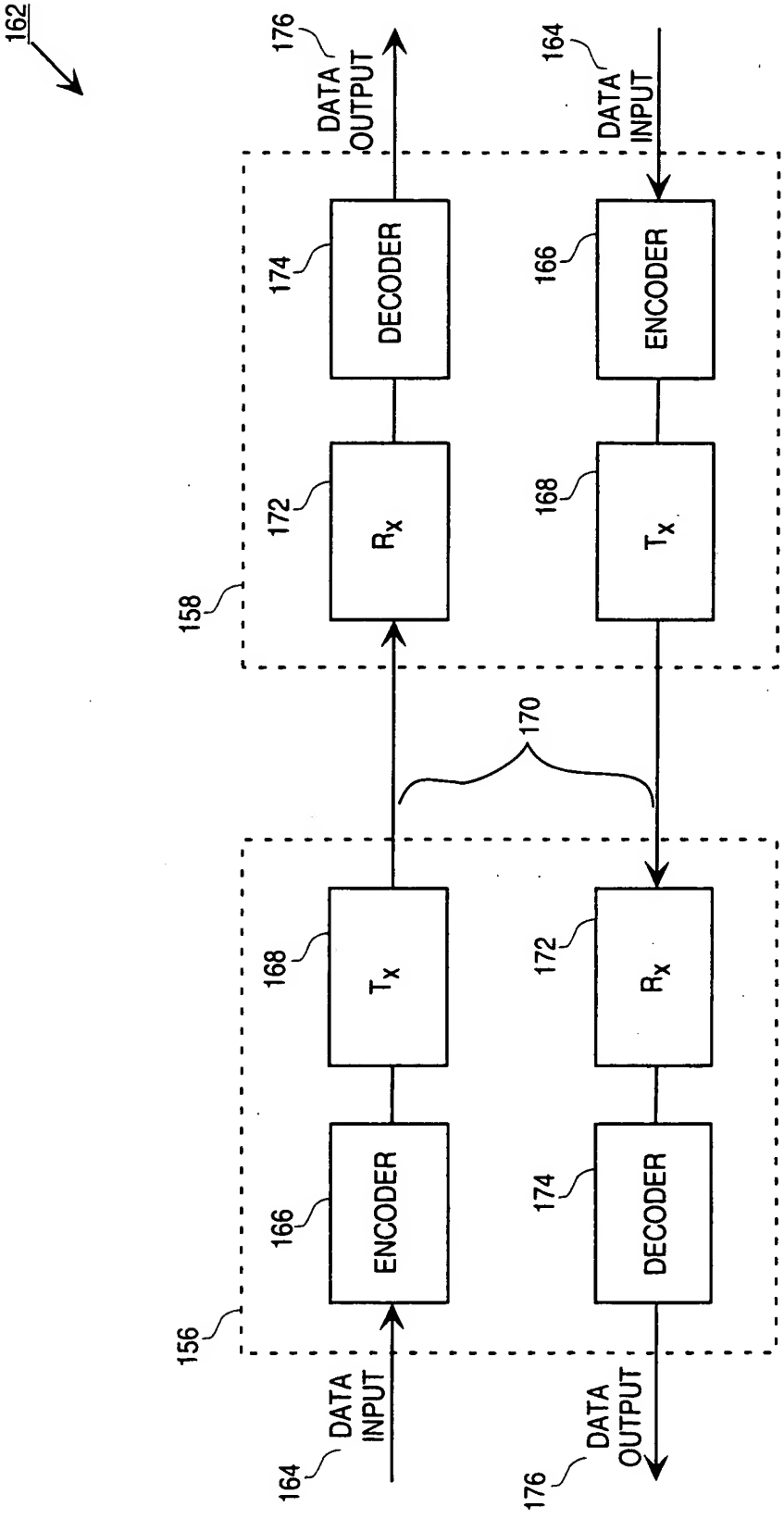

162
176
DATA OUTPUT
164
DATA INPUT
174
DECODER
166
ENCODER
172
R_x
168
T_x
158
170
168
T_x
172
R_x
166
ENCODER
174
DECODER
156
164
DATA INPUT
176
DATA OUTPUT

FIG. 8

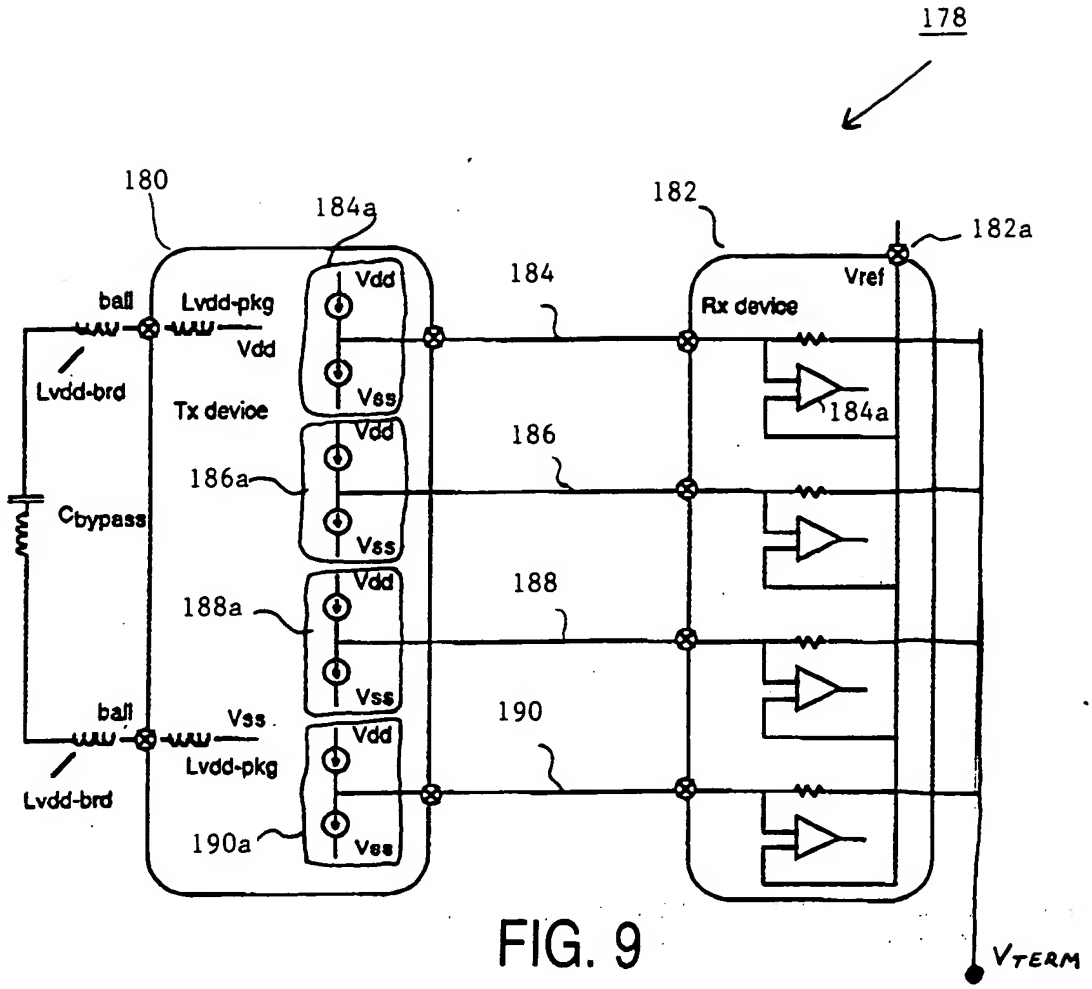

178
180
184a
182
182a
ball
Lvdd-pkg
Vdd
Vdd
Vref
184
Rx device
Lvdd-brd
Tx device
Vss
184a
Vdd
186
186a
Cbypass
Vss
Vdd
188
188a
Vss
ball
Vss
Vdd
190
Lvdd-pkg
Lvdd-brd
190a
Vss
VTERM

FIG. 9

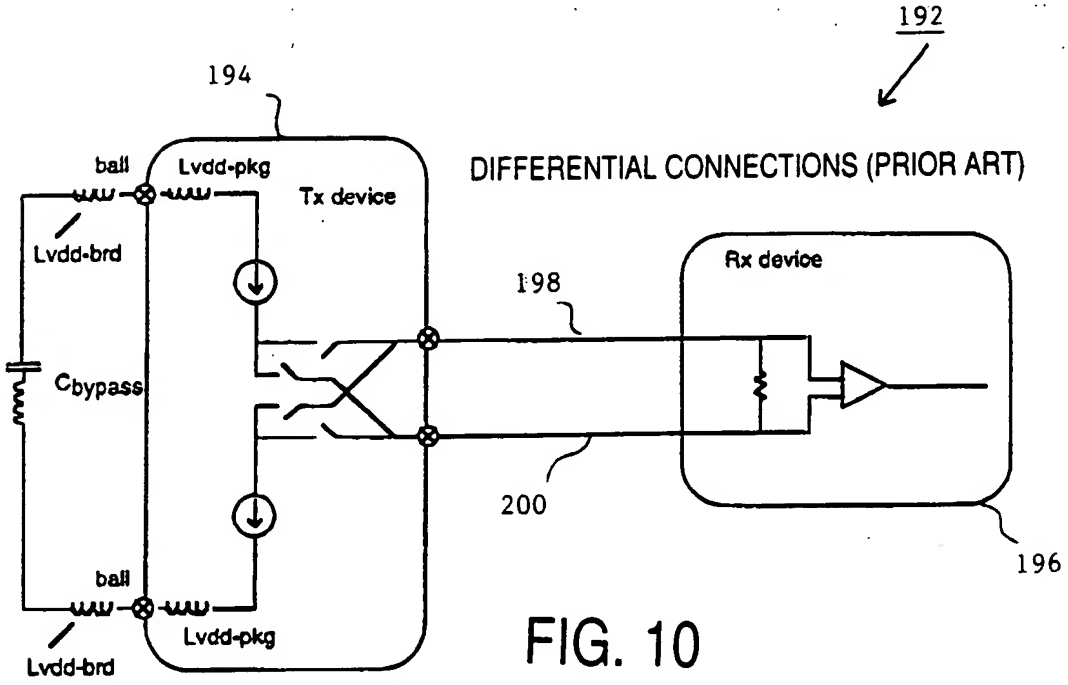

192
194
DIFFERENTIAL CONNECTIONS (PRIOR ART)
ball
Lvdd-pkg
Tx device
Lvdd-brd
Rx device
198
Cbypass
200
196
ball
Lvdd-pkg
Lvdd-brd

FIG. 10

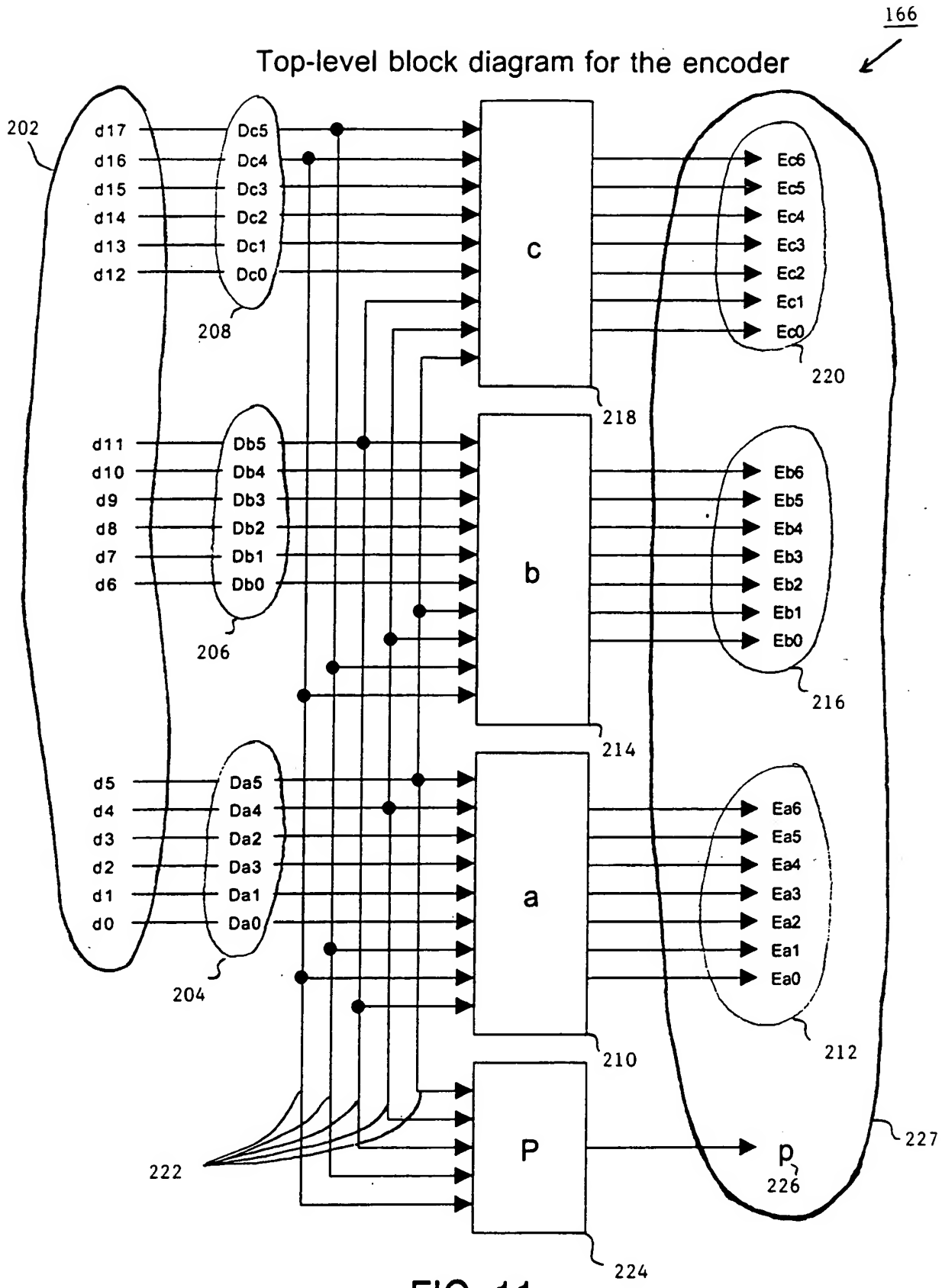

166
Top-level block diagram for the encoder
202
d17
d16
d15
d14
d13
d12
Dc5
Dc4
Dc3
Dc2
Dc1
Dc0
208
c
218
Ec6
Ec5
Ec4
Ec3
Ec2
Ec1
Ec0
220
d11
d10
d9
d8
d7
d6
Db5
Db4
Db3
Db2
Db1
Db0
206
b
214
Eb6
Eb5
Eb4
Eb3
Eb2
Eb1
Eb0
216
d5
d4
d3
d2
d1
d0
Da5
Da4
Da2
Da3
Da1
Da0
204
a
210
Ea6
Ea5
Ea4
Ea3
Ea2
Ea1
Ea0
212
222
P
224
p
226
227

FIG. 11

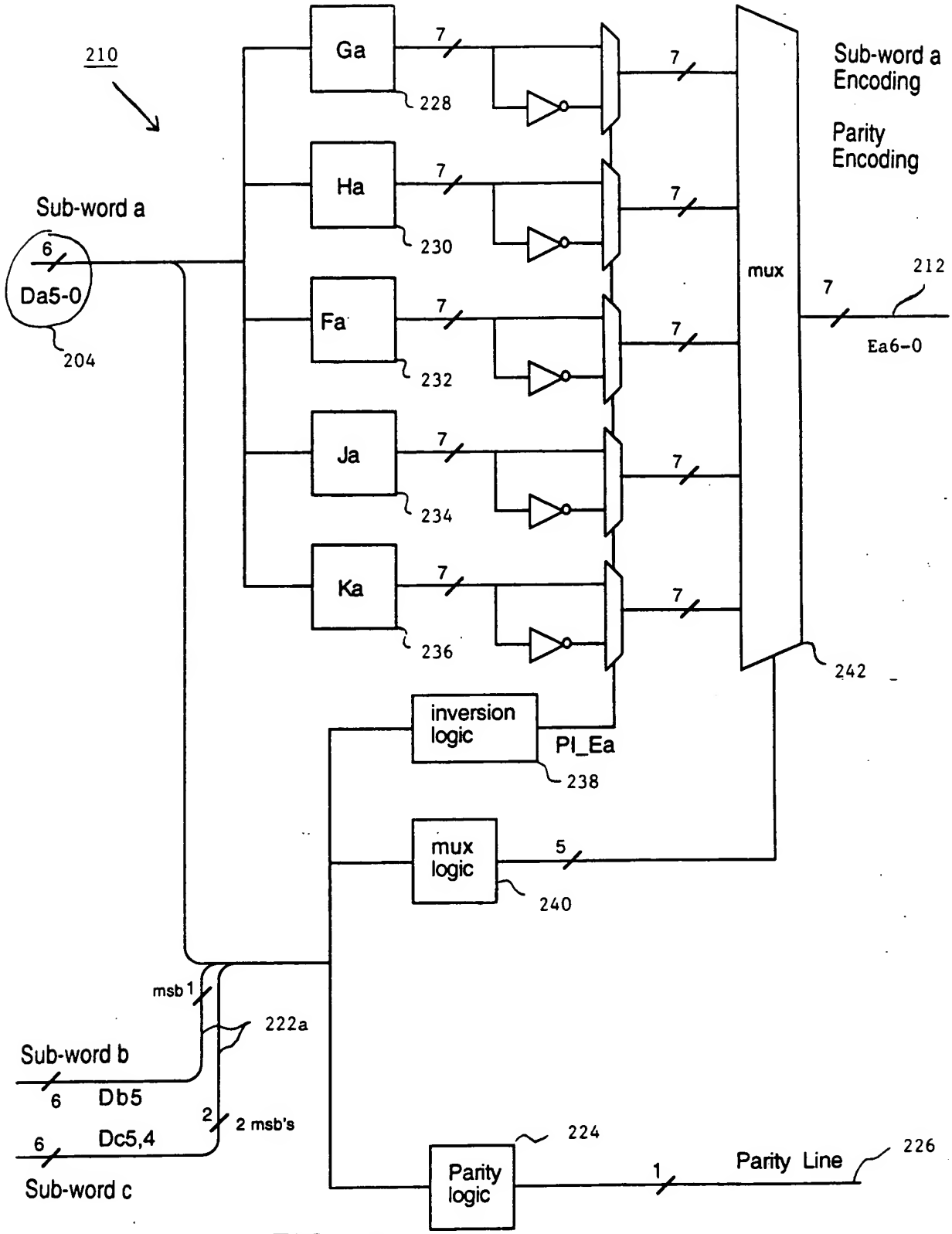

210
Sub-word a
6
Da5-0
204
Ga
228
Ha
230
Fa
232
Ja
234
Ka
236
7
mux
Sub-word a Encoding
Parity Encoding
212
Ea6-0
242
inversion logic
PI_Ea
238
mux logic
5
240
msb 1
222a
Sub-word b
6
Db5
2
2 msb's
6
Dc5,4
Sub-word c
224
Parity logic
1
Parity Line
226

FIG. 12

Encode Truth Tables for Block Diagram Elements of Sub-word a

240a

Subchannel a Mux Truth Table

Da5	Da4	Da3	Da2	Db5 + Dc5	Block
0	0	0	x	0	G
0	0	0	0	1	G
0	0	0	1	1	F1
0	0	1	x	x	J
0	1	0	x	0	K
0	1	0	x	1	J
0	1	1	x	0	H
0	1	1	x	1	K
1	0	0	x	x	J
1	0	1	x	x	K
1	1	0	x	x	K
1	1	1	0	x	F2
1	1	1	1	x	H

238a

Subch a Post Inversion Truth Table

Da5·Db5·Dc5·Dc4	Pl Ea
0	no inversion
1	invert

224a

Truth Table for Parity Bit

Da4	Da5	Db5	Dc5	Dc4	Parity Bit
0	0	0	0	x	1
1	0	0	0	x	0
x	0	0	1	x	1
x	0	1	0	x	1
x	0	1	1	x	0
x	1	0	0	x	1
x	1	0	1	x	0
x	1	1	0	x	0
x	1	1	1	0	1
x	1	1	1	1	0

Block Ga

	Da1	Da0	Ea4-0
	0	0	10000
	0	1	01000
	1	0	00100
	1	1	00010

Db5 + Dc5	Da2	Ea6	Ea5
0	0	0	1
0	1	1	0
1	x	1	1

228a

Block Ha

	Da1	Da0	Ea4-0
	0	0	11101
	0	1	11011
	1	0	10111
	1	1	01111

Db5 + Dc5	Da2	Ea6	Ea5
0	0	0	1
0	1	1	0
1	x	0	0

230a

Block Fa

	Da1	Da0	Ea4-0
	0	0	11000
	0	1	10100
	1	0	01011
	1	1	00111

Da2	Da1		Ea6	Ea5
x	0		1	
x	1		0	
0	x			1
1	x			0

232a

234a

Block Ja

	Da2	Da1	Da0	Ea4-0
	0	0	0	10010
	0	0	1	10001
	0	1	0	01100
	0	1	1	01010
	1	0	0	01001
	1	0	1	00110
	1	1	0	00101
	1	1	1	00011

Db5 + Dc5		Da4	Da3	Ea6	Ea5
0		x	x	0	0
1		x	0		1
1		x	1		0
1		0	x	1	
1		1	x	0	

Block Ka

	Da2	Da1	Da0	Ea4-0
	0	0	0	11100
	0	0	1	11010
	0	1	0	11001
	0	1	1	10110
	1	0	0	10101
	1	0	1	10011
	1	1	0	01110
	1	1	1	01101

	Da5		Da3	Ea6	Ea5
			0		1
			1		0
	0		0	1	
	0		1	0	
	1		0	0	
	1		1	1	

236a

FIG. 13

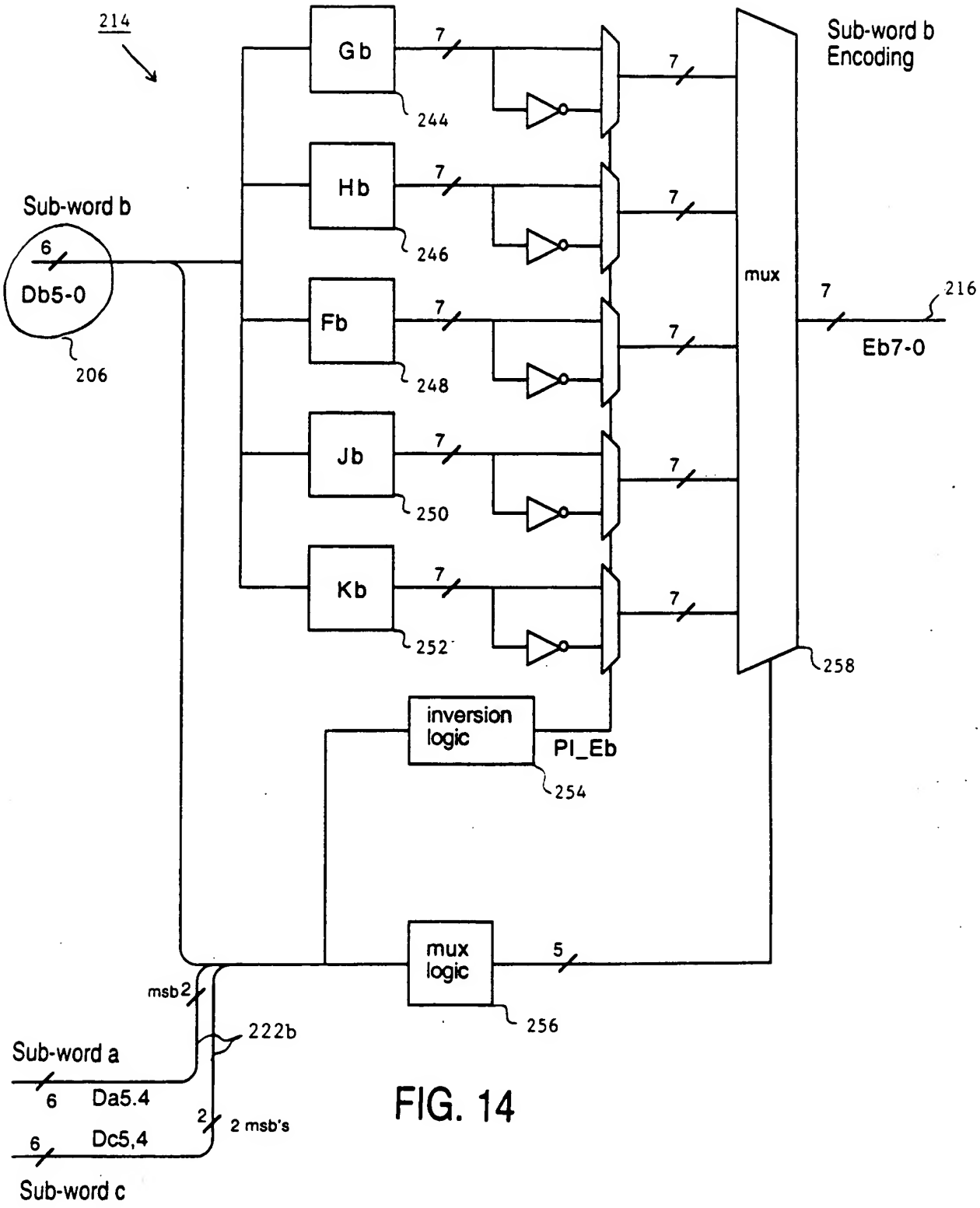

214
Gb
Hb
Fb
Jb
Kb
7
244
246
248
250
252
Sub-word b
Encoding
mux
258
216
Eb7-0
Sub-word b
6
Db5-0
206
inversion
logic
PI_Eb
254
mux
logic
5
256
msb 2
222b
Sub-word a
6
Da5.4
2
2 msb's
6
Dc5,4
Sub-word c

FIG. 14

Encode Truth Tables for Block Diagram Elements of Sub-word b

256b

Subchannel b Mux Truth Table					
Db5	Db4	Db3	Db2		Block
0	0	0	0		G
0	0	0	1		F1
0	0	1	x		J
0	1	0	x		J
0	1	1	x		K
1	0	0	x		J
1	0	1	x		K
1	1	0	x		K
1	1	1	0		F2
1	1	1	1		H

254b

Subch_b Post Inversion Truth Table					
Da4	Da5	Db5	Dc5	Dc4	Pi_Eb
0	0	0	0	x	Invert
all other combinations					no inversion
x	1	1	1	1	Invert

Block Gb			
	Db1	Db0	Eb4-0
	0	0	10000
	0	1	01000
	1	0	00100
	1	1	00010
		Eb6	Eb5
always 1 for Gb		1	1

244b

Block Hb			
	Db1	Db0	Eb4-0
	0	0	11101
	0	1	11011
	1	0	10111
	1	1	01111
		Eb6	Eb5
always 0 for Hb		0	0

246b

Block Fb				
	Db1	Db0	Eb4-0	
	0	0	11000	
	0	1	10100	
	1	0	01011	
	1	1	00111	
Db2	Db1		Eb6	Eb5
x	0		1	
x	1		0	
0	x			1
1	x			0

248b

250b

Block Jb					
	Db2	Db1	Db0	Eb4-0	
	0	0	0	10010	
	0	0	1	10001	
	0	1	0	01100	
	0	1	1	01010	
	1	0	0	01001	
	1	0	1	00110	
	1	1	0	00101	
	1	1	1	00011	
		Db4	Db3	Eb6	Eb5
		x	0		1
		x	1		0
		0	x	1	
		1	x	0	

Block Kb					
	Db2	Db1	Db0	Eb4-0	
	0	0	0	11100	
	0	0	1	11010	
	0	1	0	11001	
	0	1	1	10110	
	1	0	0	10101	
	1	0	1	10011	
	1	1	0	01110	
	1	1	1	01101	
		Db4	Db3	Eb6	Eb5
		x	0		0
		x	1		1
		0	x	1	
		1	x	0	

252b

FIG. 15

SUBSTITUTE DRAWING

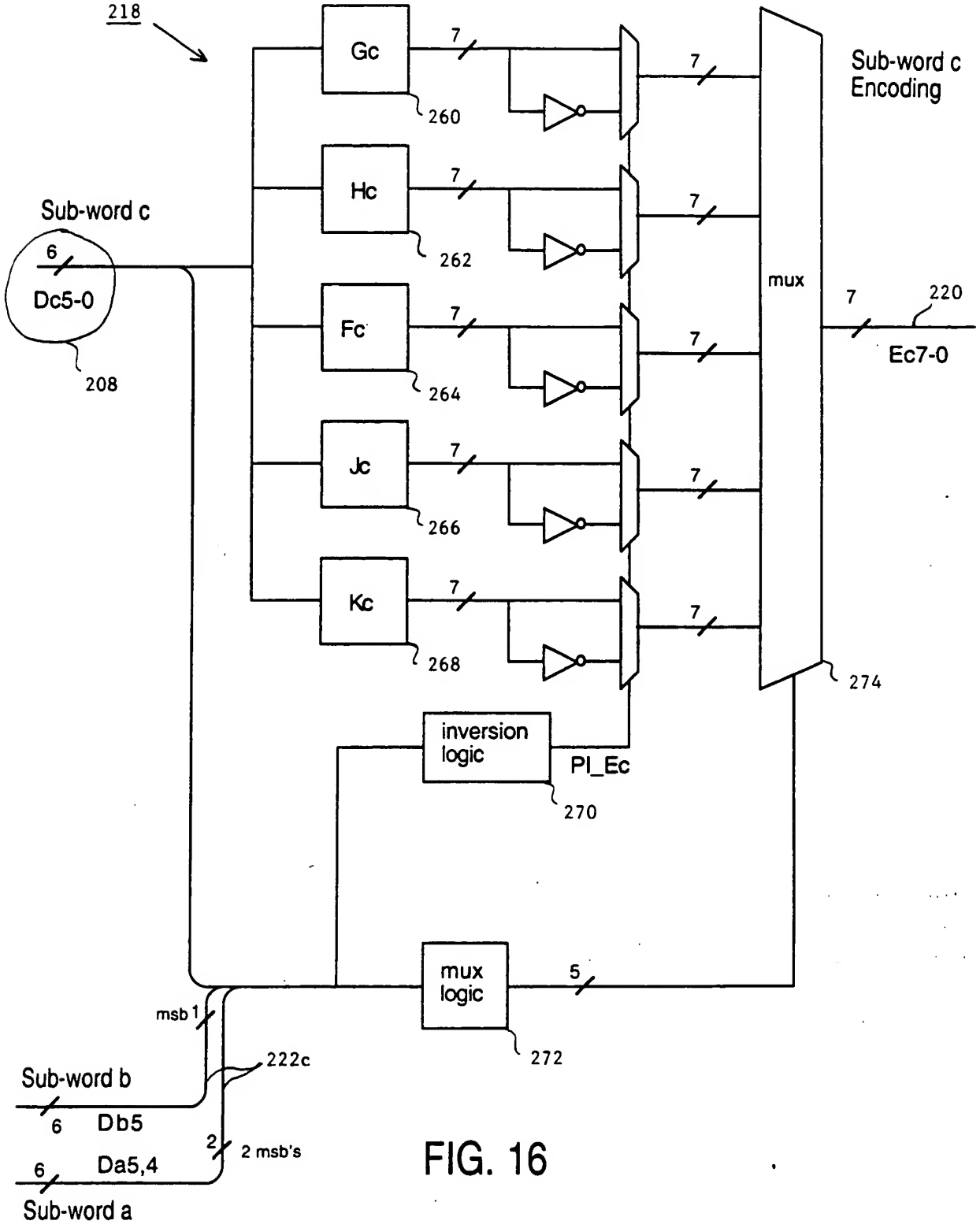

218
Gc
Hc
Fc
Jc
Kc
7
260
262
264
266
268
Sub-word c
6
Dc5-0
208
mux
Sub-word c
Encoding
220
Ec7-0
274
inversion
logic
PI_Ec
270
mux
logic
5
272
msb 1
222c
Sub-word b
6
Db5
2
2 msb's
6
Da5,4
Sub-word a

FIG. 16

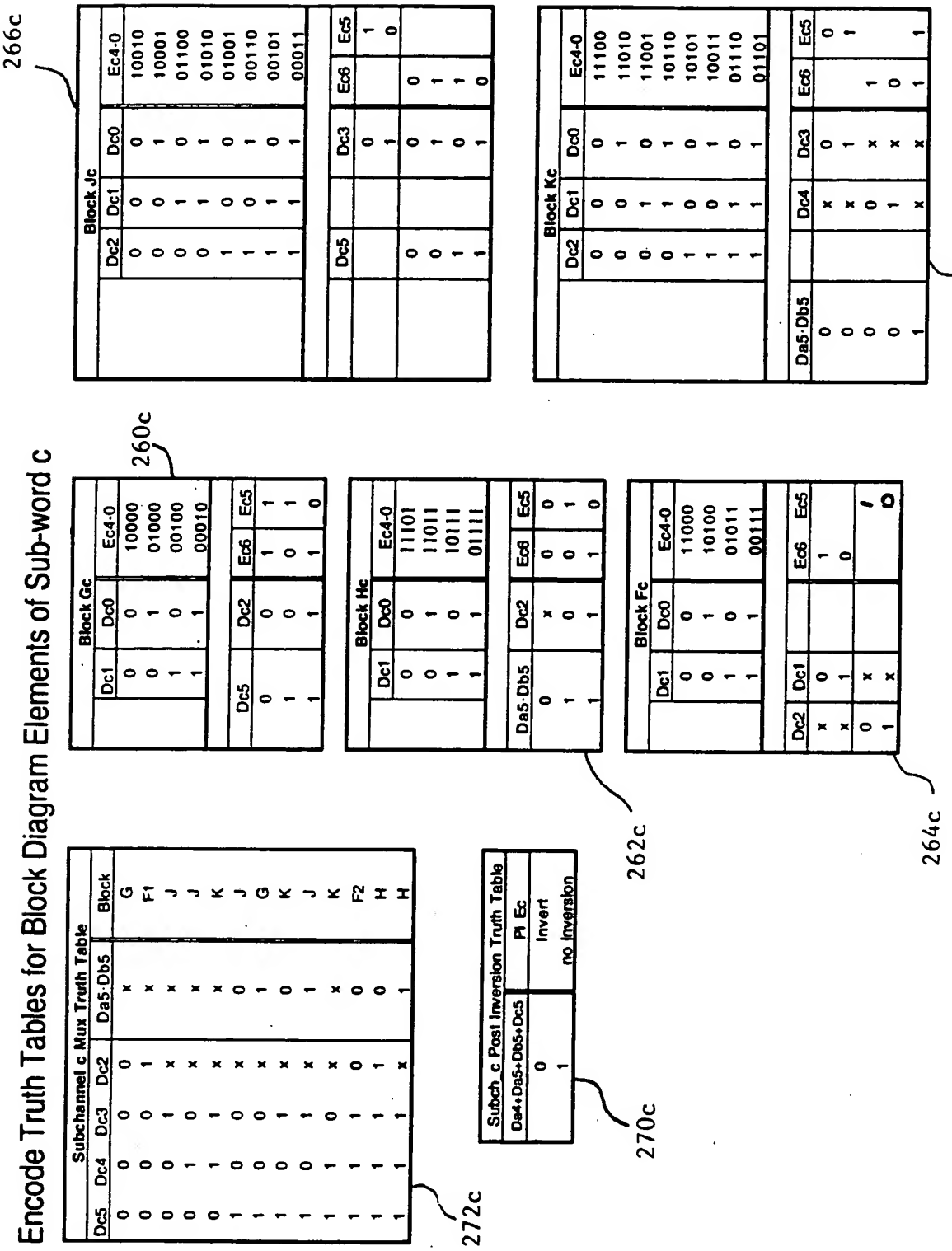

Encode Truth Tables for Block Diagram Elements of Sub-word c
Subchannel c Mux Truth Table
Dc5 Dc4 Dc3 Dc2 Da5·Db5 Block
G
F1
J
J
K
J
G
K
J
K
F2
H
H
272c
Subch_c Post Inversion Truth Table
Da4+Da5+Db5+Dc5
P1 Ec
0 Invert
1 no inversion
270c
260c
Block Gc
Dc1 Dc0 Ec4-0
10000
01000
00100
00010
Dc5 Dc2 Ec6 Ec5
Block Hc
Dc1 Dc0 Ec4-0
11101
11011
10111
01111
Da5·Db5 Dc2 Ec6 Ec5
262c
Block Fc
Dc1 Dc0 Ec4-0
11000
10100
01011
00111
Dc2 Dc1 Ec6 Ec5
264c
266c
Block Jc
Dc2 Dc1 Dc0 Ec4-0
10010
10001
01100
01010
01001
00110
00101
00011
Dc5 Dc3 Ec6 Ec5
Block Kc
Dc2 Dc1 Dc0 Ec4-0
11100
11010
11001
10110
10101
10011
01110
01101
Da5·Db5 Dc4 Dc3 Ec6 Ec5
268c

FIG. 17

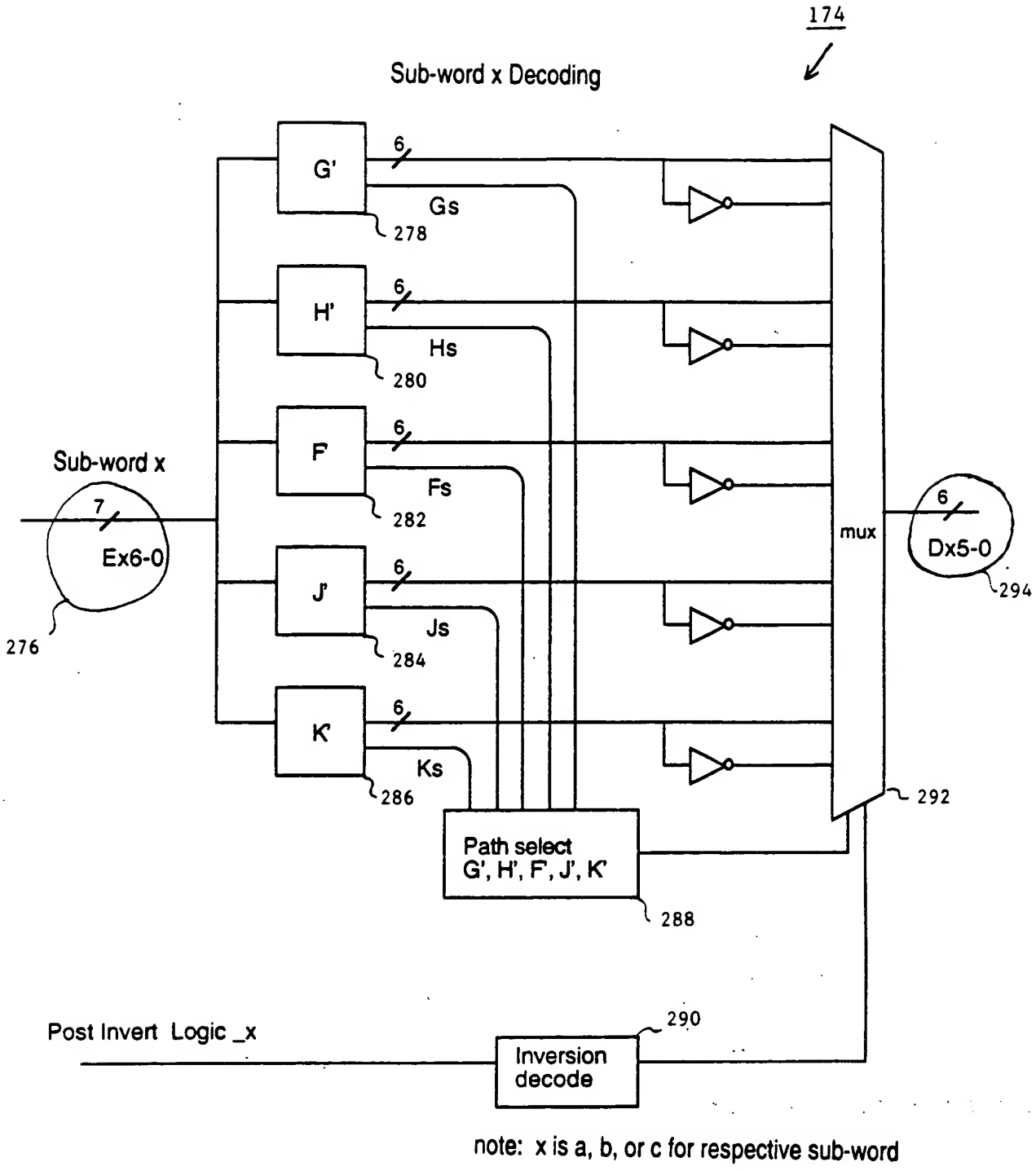

174
Sub-word x Decoding
G'
6
Gs
278
H'
6
Hs
280
F'
6
Fs
282
J'
6
Js
284
K'
6
Ks
286
Sub-word x
7
Ex6-0
276
mux
6
Dx5-0
294
292
Path select
G', H', F', J', K'
288
Post Invert Logic _x
290
Inversion
decode
note: x is a, b, or c for respective sub-word

FIG. 18

296

Truth Table for Sub-word a Decode

Decode Mux Truth Table Sub-word a

	Decode Path Mux Control											
Ea4-0	Gas	Has	Fas	Jas	Kas	Block	Da5	Da4	Da3	Da2	Da1	Da0	
10000	1	0	0	0	0	G′	0	0	0	Ea5_	0	0	278a
01000	1	0	0	0	0	G′	0	0	0	Ea5_	0	1	
00100	1	0	0	0	0	G′	0	0	0	Ea5_	1	0	
00010	1	0	0	0	0	G′	0	0	0	Ea5_	1	1	
11101	0	1	0	0	0	H′	Ea6_·Ea5_	1	1	Ea5_	0	0	280a
11011	0	1	0	0	0	H′	Ea6_·Ea5_	1	1	Ea5_	0	1	
10111	0	1	0	0	0	H′	Ea6_·Ea5_	1	1	Ea5_	1	0	
01111	0	1	0	0	0	H′	Ea6_·Ea5_	1	1	Ea5_	1	1	
11000	0	0	1	0	0	F′	Ea5	Ea5	Ea5	Ea5_	0	0	282a
10100	0	0	1	0	0	F′	Ea5	Ea5	Ea5	Ea5_	0	1	
01011	0	0	1	0	0	F′	Ea5	Ea5	Ea5	Ea5_	1	0	
00111	0	0	1	0	0	F′	Ea5	Ea5	Ea5	Ea5_	1	1	
10010	0	0	0	1	0	J′	Ea5·Ea6	Ea6_·Ea5	Ea5_	0	0	0	284a
10001	0	0	0	1	0	J′	Ea5·Ea6	Ea6_·Ea5	Ea5_	0	0	1	
01100	0	0	0	1	0	J′	Ea5·Ea6	Ea6_·Ea5	Ea5_	0	1	0	
01010	0	0	0	1	0	J′	Ea5·Ea6	Ea6_·Ea5	Ea5_	0	1	1	
01001	0	0	0	1	0	J′	Ea5·Ea6	Ea6_·Ea5	Ea5_	1	0	0	
00110	0	0	0	1	0	J′	Ea5·Ea6	Ea6_·Ea5	Ea5_	1	0	1	
00101	0	0	0	1	0	J′	Ea5·Ea6	Ea6_·Ea5	Ea5_	1	1	0	
00011	0	0	0	1	0	J′	Ea5·Ea6	Ea6_·Ea5	Ea5_	1	1	1	
11100	0	0	0	0	1	K′	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	0	0	0	286a
11010	0	0	0	0	1	K′	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	0	0	1	
11001	0	0	0	0	1	K′	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	0	1	0	
10110	0	0	0	0	1	K′	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	0	1	1	
10101	0	0	0	0	1	K′	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	1	0	0	
10011	0	0	0	0	1	K′	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	1	0	1	
01110	0	0	0	0	1	K′	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	1	1	0	
01101	0	0	0	0	1	K′	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	1	1	1	

Post Inversion Logic

Invert Results of sub-word a decode if W5subCh_c =1

Invert decoded value for sub-word a if the weight of sub-word c equals 5

290a

FIG. 19

298

Decode Mux Truth Table Sub-word b

	Decode Path Mux Control												
Eb4-0	Gbs	Hbs	Fbs	Jbs	Kbs	Block		Db5	Db4	Db3	Db2	Db1	Db0
10000	1	0	0	0	0	G′		0	0	0	0	0	0
01000	1	0	0	0	0	G′		0	0	0	0	0	1
00100	1	0	0	0	0	G′		0	0	0	0	1	0
00010	1	0	0	0	0	G′		0	0	0	0	1	1
11101	0	1	0	0	0	H′		1	1	1	1	0	0
11011	0	1	0	0	0	H′		1	1	1	1	0	1
10111	0	1	0	0	0	H′		1	1	1	1	1	0
01111	0	1	0	0	0	H′		1	1	1	1	1	1
11000	0	0	1	0	0	F′		Eb5	Eb5	Eb5	Eb5_	0	0
10100	0	0	1	0	0	F′		Eb5	Eb5	Eb5	Eb5_	0	1
01011	0	0	1	0	0	F′		Eb5	Eb5	Eb5	Eb5_	1	0
00111	0	0	1	0	0	F′		Eb5	Eb5	Eb5	Eb5_	1	1
10010	0	0	0	1	0	J′		Eb5·Eb6	Eb6_	Eb5_	0	0	0
10001	0	0	0	1	0	J′		Eb5·Eb6	Eb6_	Eb5_	0	0	1
01100	0	0	0	1	0	J′		Eb5·Eb6	Eb6_	Eb5_	0	1	0
01010	0	0	0	1	0	J′		Eb5·Eb6	Eb6_	Eb5_	0	1	1
01001	0	0	0	1	0	J′		Eb5·Eb6	Eb6_	Eb5_	1	0	0
00110	0	0	0	1	0	J′		Eb5·Eb6	Eb6_	Eb5_	1	0	1
00101	0	0	0	1	0	J′		Eb5·Eb6	Eb6_	Eb5_	1	1	0
00011	0	0	0	1	0	J′		Eb5·Eb6	Eb6_	Eb5_	1	1	1
11100	0	0	0	0	1	K′		Eb6 + Eb5	Eb6_	Eb5_	0	0	0
11010	0	0	0	0	1	K′		Eb6 + Eb5	Eb6_	Eb5_	0	0	1
11001	0	0	0	0	1	K′		Eb6 + Eb5	Eb6_	Eb5_	0	1	0
10110	0	0	0	0	1	K′		Eb6 + Eb5	Eb6_	Eb5_	0	1	1
10101	0	0	0	0	1	K′		Eb6 + Eb5	Eb6_	Eb5_	1	0	0
10011	0	0	0	0	1	K′		Eb6 + Eb5	Eb6_	Eb5_	1	0	1
01110	0	0	0	0	1	K′		Eb6 + Eb5	Eb6_	Eb5_	1	1	0
01101	0	0	0	0	1	K′		Eb6 + Eb5	Eb6_	Eb5_	1	1	1

278b

280b

282b

284b

286b

Post Inversion Logic

Invert Results of sub-word _b decode if W5subCh_c + W2subCh_a =1
W5subCh_c = Kcs·Ec6·Ec5 + Hcs·(Ec6 + Ec5)
W2subCh_a = Jas·Ea6_·Ea5_ + Gas·(Ea6_ + Ea5_)

Invert decoded value for sub-word b if the weight of sub-word c = 5 and/or the weight of sub-word a = 2

290b

FIG. 20

300

Decode Mux Truth Table Sub-word c

Ec4-0	Decode Path Mux Control Gcs	Hcs	Fcs	Jcs	Kcs	Block	Dc5	Dc4	Dc3	Dc2	Dc1	Dc0	
10000	1	0	0	0	0	G′	Ec6_+Ec5_	0	0	Ec5_	0	0	278c
01000	1	0	0	0	0	G′	Ec6_+Ec5_	0	0	Ec5_	0	1	
00100	1	0	0	0	0	G′	Ec6_+Ec5_	0	0	Ec5_	1	0	
00010	1	0	0	0	0	G′	Ec6_+Ec5_	0	0	Ec5_	1	1	
11101	0	1	0	0	0	H′	1	1	1	Ec5_	0	0	280c
11011	0	1	0	0	0	H′	1	1	1	Ec5_	0	1	
10111	0	1	0	0	0	H′	1	1	1	Ec5_	1	0	
01111	0	1	0	0	0	H′	1	1	1	Ec5_	1	1	
11000	0	0	1	0	0	F′	Ec5	Ec5	Ec5	Ec5_	0	0	282c
10100	0	0	1	0	0	F′	Ec5	Ec5	Ec5	Ec5_	0	1	
01011	0	0	1	0	0	F′	Ec5	Ec5	Ec5	Ec5_	1	0	
00111	0	0	1	0	0	F′	Ec5	Ec5	Ec5	Ec5_	1	1	
10010	0	0	0	1	0	J′	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	0	0	0	284c
10001	0	0	0	1	0	J′	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	0	0	1	
01100	0	0	0	1	0	J′	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	0	1	0	
01010	0	0	0	1	0	J′	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	0	1	1	
01001	0	0	0	1	0	J′	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	1	0	0	
00110	0	0	0	1	0	J′	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	1	0	1	
00101	0	0	0	1	0	J′	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	1	1	0	
00011	0	0	0	1	0	J′	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	1	1	1	
11100	0	0	0	0	1	K′	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	0	0	0	286c
11010	0	0	0	0	1	K′	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	0	0	1	
11001	0	0	0	0	1	K′	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	0	1	0	
10110	0	0	0	0	1	K′	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	0	1	1	
10101	0	0	0	0	1	K′	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	1	0	0	
10011	0	0	0	0	1	K′	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	1	0	1	
01110	0	0	0	0	1	K′	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	1	1	0	
01101	0	0	0	0	1	K′	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	1	1	1	

Post Inversion Logic

Invert Results of sub-word b decode if W2subCh_a =1

W2subCh_a = Jas·Ea6_·Ea5_ + Gas·(Ea6_ + Ea5_)

Invert decoded value for sub-word c if the weight of sub-word a = 2

290c

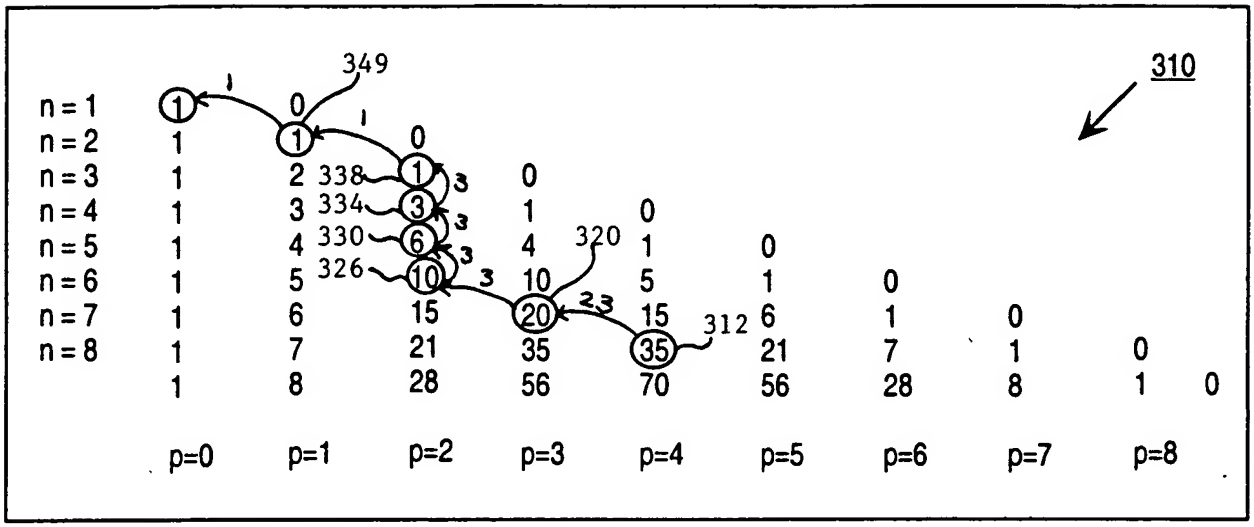
FIG. 21

302

(4B/6L EXAMPLE)
CORRESPONDENCE BETWEEN
DECIMAL, BINARY, AND ENCODED VALUES

304	306	308
DECIMAL VALUE	BINARY VALUE	ENCODED VALUE
DECIMAL COUNT	BINARY COUNT	BINOMIAL COUNT
0	0000	000111
1	0001	001011
2	0010	001101
3	0011	001110
4	0100	010011
5	0101	010101
6	0110	010110
7	0111	011001
8	1000	011010
9	1001	011100
10	1010	100011
11	1011	100101
12	1100	100110
13	1101	101001
14	1110	101010
15	1111	101100
16	EXTRA	110001
17	EXTRA	110010
18	EXTRA	110100
19	EXTRA	111000

FIG. 22



$$n_p = \frac{(n\ (n-1)\ (n-2)\ .\ .\ .\ .\ n-[p-1])}{1 \cdot 2 \cdot 3 \ldots . p}$$

310a

$58_{10} = 11000110$

310b

FIG. 23